**BS Map SD UHS-I**

BS0------COMMAND reg. 1 byte, W,

**0 - Start, 1=STC, 2=PRG State Detection, 3= CRC7\_Reversed, 4= , 5=CRCS\_ER\_EN, 6=CRC16\_REV, 7=**

BS1------STATUS tester 2 By R, **0=run, 1 = End, 2=ERR\_CRCS, 3=, 4=ERD, 5=ERCRC7, 6=EDS\_OFL, 7=STOP uC(eMMC+UHS-I),**

**8=TO\_R1, 9=TO\_R2, 10=TO\_RDY, 11=TO\_ACP, 12 = ERR\_CRC16, 13=AD\_ERR/WP Violation, 14=D0\_State, 15=TO\_R3,**

BS2-------Read Error CRC16 (CRC16\_ER0, 1,…,7), 1 Byte R

BS3-------Program Counter state; 1 byte, R

BS4-------Read CRC16; 16 bytes Read, SDR 8bits x 2 Bytes / CRC16 = 16 Bytes **(N/A in DDR designs)**

BS5-------Read CRC Status (5 bits), R (on DL from the card)

BS6-------MicroProgram Memory, 512x12 bytes= 6 KB, W (3 x RAMB18SDP)

BS7-------Error Counter, 5 bytes, Read, *LSB first*

BS8-------Watchdog, 5 bytes Read, *LSB first*

BS9-------Read CRC7 from Response, 1 byte, R

BS10------Read Index from Response, 1 byte Read

BS11------Delete Status / Control LED, 1 byte W, **00=delete** Status, **01=Del. St. & Green** (Pass),

**02=Del. St. & Red** (Error), **04=Del. St. & Green Flashing** (End all tests)

BS12------Enable Clock DUT stop, 1 byte W, **01 = Stop clock enable (Tester+DUT), 02=Enable Stop DUT Clock**

BS13------RSP, 1 byte, Write

**BS14**------(*MSB first*) RCA Register, 2x4 bytes, W

BS15------(*MSB first*) Status Card read (RCA & Status CMD3\_ SD), 16x4 bytes, R

**BS16**------(*MSB first*) OCR Register, 4 bytes, R / W

BS17------CID/CSD, 2x16 bytes, R, CID/CSD value as R2 to **CMD2/9/10**, 16 bytes W, CID/CSD Reg as ARG **CMD26/27**

BS18------**Buffer Memory WRITE**, W, 32 KB for a Block Data to be written in DUT (8 x RAMB36)

BS19------**eMMC >** RST\_n (Hardware Reset), W 1 Byte, 01 / 00

BS20------**Buffer Memory READ**, Read, 32 KB for Block read from DUT (8 x RAMB36)

**BS21------Data Pattern Read for DDR Mode, 8 Bytes Read**

BS22------Error Buffer Memory, Read, 4K x 4 Byte (4 Byte Address) (4 x RAMB18)

BS23------Number of Defective Block, Read 2 Bytes (max. 2\*\*16 blocks)

**BS24------Data Pattern P4B**, Write 4 bytes, Read – last 16 bytes

**BS25------(*MSB first*) R/W Address, 4Kx4 bytes (4 Byte Address),** Write (4xRAMB36)

BS26------Status Card Addr., R nr. of cards sent R1 to CMD3(MMC) & R2 to CMD2, W 1 byte, Addr. of Status Mem 16x4

BS27------DLL Phase Control, CLK\_DUT, **W ff=shift right**, **W 00=shift left**

BS28------DLL Reset, **W** **ff/00**

BS29------Byte Counter (for Stream Read/Write, Block Length Read/Write), 4 bytes, Write

**WSB / RSB=01 fe ff ff ; 512 bytes Block Length**

### W\_Stream / R\_Stream / 1BL=01 fe ff ff , 2BL=1K=01 fc ff ff, 16BL=8K=01 e0 ff ff, 2\*\*15BL=16M=01 00 00 ff

BS30-------Block Counter (Multiple Block Read/Write), 4 bytes, Write

**1 BLK=ff ff ff ff, 2BLK=fe ff ff ff, 8BLK=f8 ff ff ff, 2\*\*11 blocks= 1MB=00 f8 ff ff**

**2\*\*15 blocks= 16MB=00 80 ff ff, 2\*\*17 blocks= 64MB=00 00 fe ff, 2\*\*20 blocks= 512MB=00 00 f0 ff**

BS31------Time-out1 Cnter, “TO\_R3” (for busy R3), 2 bytes, W (**00 fc ~ 1 sec.), TO\_PRG\_State, Nr of repeated CMD13**

BS32------Time-out2 Counter, “TOAC” (for NAC & Programming), 4 bytes, W (**00 00 ff ff= 1sec/20 MHz**)

## BS33------Stop Counter (for Stop Transmission), 4 bytes W, 01 fe ff ff ; 512 bytes Block Length

## BS34------General Purpose Counter GPCI, 4 bytes W, for Performance test, 2s complement *LSB first* of Nr of Random Add Blocks

BS35------**R1 for ROM\_RSB, RMB, R\_Stream**, 6 bytes Read

BS36------(*MSB first*)Block Length (Read/Write), 4 bytes, W (**512 bytes=00 00 02 00)**

BS37------(*MSB first*) Block Count, W 4 Bytes, **00 00 00 00 = 0 blocks; 00 00 00 01 = 1 block; 00 00 00 03 = 3 blocks;**

**00 00 08 00=2\*\*11=1MB, 00 00 80 00=2\*\*15=16MB, 00 01 00 00=2\*\*16 blks=32MB**

BS38------Time-out NCR Counter, 1 byte W (c0 = 64 cycles, 00 = 256 cycles)

BS39------*HS-MMC, Reset to 1 Bit Mode*

BS40------Option Reg, 1 byte W, **01=prevent STARTM, 02=prevent Led Test from ST0/Led Test Off, 06 Led Test on**

BS41------Read CD & WP (card detect & write protect), 1 byte, R

**BS42------Power Stop Timer controlled by uCode, Write 2 Bytes, MSB first, 01 00 >> SP\_VIR4=1 after 256 SCK, 7.23.13**

**BS43**------Clock Divider, W 1Byte**: 00 = 20MHz; 04 = 4MHz; 07 = 2.73MHz; 13 = 1MHz; 31 = 400KHz; 73 = 170KHz**

BS44------Frequency DUT, 4 bytes, W

BS96(32)-------PERFORMANCE mode, W 1 Byte, 00 = Normal, 01 = Performance (MUX for Block Counter)

**BS97(33)-------Block Cnter Memory (BS30)**, W 1K x 4 By >> ff ff ff ff= 1 Block, fe ff ff ff=2 Blocks, 00 ff ff ff=256 Blks, (1xRAMB36)

00 00 ff ff=64K Blks 00 00 00 ff=16M Blks

BS98(34)-------**WATCHDOG Buffer,** Read 2K x 4 Bytes *(MSB first)* (4xRAMB18)

BS99(35)-------**Loop Counter**, W 2 bytes *(2s complement, LSB),* **ff ff = 1 loop, f0 ff = 16 loops**

BS100(36)------**Gen Purpose Counter (BS34) Memory**, W 2Kx16, ff ff = 1 loop, fe ff = 2 loops (1xRAMB36)

BS101(37)------Read Address of WATCHDOG Buffer, R 2 Bytes *(MSB first)*

BS102(38)------**MAX THROUGHPUT,** R 4 Bytes *(MSB first, in Number of Clocks)*

BS103(39)------**Min THROUGHPUT,** R 4 Bytes *(MSB first, in Number of Clocks)*

BS104(40)------**Min Write LATENCY,** R 4 Bytes *(MSB first, in Number of Clocks)*

BS105(41)------**MAX Write LATENCY,** R 4 Bytes *(MSB first, in Number of Clocks)*

BS106(42)------**Min Read LATENCY,** R 4 Bytes *(MSB first, in Number of Clocks)*

BS107(43)------**MAX Read LATENCY,** R 4 Bytes *(MSB first, in Number of Clocks)*

BS108(44)------**Average Write LATENCY,** R 5 Bytes *(MSB first, in Number of Clocks)*

BS109(45)------**Average Read LATENCY,** R 5 Bytes *(MSB first, in Number of Clocks)*

BS110(46)------**WSB Random Address Buffer,** W 1K x 4 Bytes *(MSB first)*